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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/593,446	09/19/2006	Yoshitaka Kinoshita	071971-0741	9940
53080 7590 10/14/2009 MCDERMOTT WILL & EMERY LLP 600 13TH STREET, NW WASHINGTON, DC 20005-3096				
EXAMINER				
WEBB, VERNON P				
ART UNIT		PAPER NUMBER		
2811				
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/593,446

**Applicant(s)**

KINOSHITA ET AL.

**Examiner**

VERNON P. WEBB

**Art Unit**

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 17 September 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-9, 11, 12 and 14-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 20 is/are allowed.
- 6) ☒ Claim(s) 1-9, 11, 12, 14, 19 and 21 is/are rejected.
- 7) ☒ Claim(s) 15-18 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 September 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

### ***DETAILED ACTION***

#### ***Status of Application***

1. This office action is in response to the filing of the amendment on 14 October 2008, Claims 1-9, 11, 12, and 14-21 are pending in this application.

#### ***Response to Arguments***

2. Applicant's arguments see Applicant Arguments/Remarks, filed 09/17/2009, with respect to claims 1-9, 11, 12, and 14-20 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Hasegawa et al. (U.S. Pub. Application 2005/0269584 A1) further in view of Tsujimura et al. (U.S. Pub. Application 2003/0168653 A1) and Nido (U.S. Pat. 5,793,054 A).

#### ***Allowable Subject Matter***

3. Claims 15-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

#### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
  2. Ascertaining the differences between the prior art and the claims at issue.
  3. Resolving the level of ordinary skill in the pertinent art.
  4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
3. Claims 1-9, 11, 12, 14, 19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al. (U.S. Pub. Application 2004/0147134 A1) further in view of Tsujimura et al. (U.S. Pub. Application 2003/0168653 A1) and Nido (U.S. Pat. 5,793,054 A).
4. Regarding claim 1, Hasegawa et al. discloses a light-emitting diode comprising:
- a light-emitting layer (item 16) formed over the first n-type semiconductor layer (pg. 3, paragraph [0048]; Figs. 1-9).
  - a second n-type semiconductor layer (item 12) formed between the substrate (item 11) and the first n-type semiconductor layer (item 13) (pg. 3, paragraph [0046]; Figs. 1-9);
  - a third n-type semiconductor layer (item 14) formed between the first n-type semiconductor layer (item 13) and the light-emitting layer (item 16) (pg. 3, paragraph [0046]; Figs. 1-9).
5. Hasegawa et al. does not disclose a light-emitting diode a substrate made of group III-V nitride semiconductor or a first n-type semiconductor layer containing indium and formed over a main surface of the substrate.

6. However Tsujimura et al. discloses a light-emitting diode comprising a substrate (item 11) made of group III-V nitride semiconductor (pg. 4, paragraph [0071]; Fig. 1).
7. Additionally Nido discloses a light-emitting diode comprising a first n-type semiconductor layer (item 3) containing indium and formed over a main surface of the substrate (item 1) (col. 7, lines 29-45; Fig. 1).
8. It would have been obvious for one of ordinary skill in the art to form a light-emitting diode as disclosed by Hasegawa, comprising a substrate made of group III-V nitride semiconductor as disclosed by Tsujimura et al. and a first n-type semiconductor layer containing indium and formed over a main surface of the substrate as disclosed by Nido since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.
9. Regarding claim 2, Hasegawa et al. as modified by Tsujimura et al. discloses a diode as described in reference to claim 1, wherein the substrate (item 11) is made of gallium nitride (pg. 4, paragraph [0071]; Fig. 1; same motivation).
10. Regarding claim 3, Hasegawa et al. discloses a diode as described in reference to claim 1, wherein the substrate (item 11) is a substrate whose main surface is polished (pg. 3, paragraph [0044]; Figs. 1-9).
11. Regarding claim 4, Hasegawa et al. discloses a diode as described in reference to claim 3, wherein the substrate (item 11) is a substrate whose main surface is etched (pg. 3, paragraph [0044]; Figs. 1-9).

12. Regarding claim 5, Hasegawa et al. discloses a diode as described in reference to claim 3, wherein the substrate (item 11) is a substrate whose main surface is planarized (pg. 3, paragraphs [0044-0045]; Figs. 1-9).

13. Regarding claim 6, Hasegawa et al. discloses a diode as described in reference to claim 1, wherein the light-emitting layer (item 16) has a multiple quantum well structure (item 15) formed by alternately stacking a quantum well layer and a barrier layer, and the quantum well layer has a thickness of 1 to 2.5 nm inclusive (pg. 3, paragraph [0047]; Figs. 1-9)

14. Regarding claim 7, Hasegawa et al. as modified by Sato et al. discloses a diode as described in reference to claim 1, wherein the first n-type semiconductor layer is made of a compound whose general formula is represented by  $\text{In}_a\text{Al}_b\text{Ga}_{1-a-b}\text{N}$  ( $0 < a < 1$ ,  $0 \leq b < 1$ ,  $a+b \leq 1$ ) (col. 8, lines 35-39; Fig. 1; same motivation).

15. Regarding claim 8, Hasegawa et al. discloses a diode as described in reference to claim 7, wherein the aluminum content of the first n-type semiconductor layer (item 13) is 3% or lower (pg. 3, paragraph [0046]; Figs. 1-9).

16. Regarding claim 9, Hasegawa et al. discloses a diode as described in reference to claim 1, wherein the first n-type semiconductor layer (item 13) has a thickness of 10 nm to 1  $\mu\text{m}$  inclusive (pg. 3, paragraph [0046]; Figs. 1-9).

17. Regarding claim 11, Hasegawa et al. discloses a diode as described in reference to claim 10, wherein the second n-type semiconductor layer (item 12) is made of a compound whose general formula is represented by  $\text{In}_c\text{Al}_d\text{Ga}_{1-c-d}\text{N}$  ( $0 \leq c < 1$ ,  $0 \leq d < 1$ ,  $c+d < 1$ ) (pg. 3, paragraph [0046]; Figs. 1-9).

18. Regarding claim 12, Hasegawa et al. discloses a diode as described in reference to claim 11, wherein the second n-type semiconductor layer (item 12) is an n-type contact layer (pg. 3, paragraph [0044]; Figs. 1-9).

19. Regarding claim 14, Hasegawa et al. discloses a diode as described in reference to claim 13, wherein the third n-type semiconductor layer (item 14) is an n-type contact layer (pg. 3, paragraph [0046]; Figs. 1-9).

20. Regarding claim 19, Hasegawa et al. discloses diode as described in reference to claim 1, further comprising:

- an n-type contact layer (item 12) which is formed between the substrate (item 11) and the light-emitting layer (item 16) and a portion of which is exposed (pg. 3, paragraph [0046]; Figs. 1-9);
- an n-side electrode (item 23) formed on the exposed portion of the n-type contact layer (item 12) (pg. 4, paragraph [0062]; Figs. 1-9);
- an n-type cladding layer (item 14) formed between the first n-type semiconductor layer (item 13) and the light-emitting layer (item 16) (pg. 3, paragraph [0046]; Figs. 1-9);
- a p-type semiconductor layer (item 17) formed on the light-emitting layer (item 16) (pg. 3, paragraph [0048]; Figs. 1-9);
- a p-side electrode (item 98) formed over the p-type semiconductor layer (item 17), wherein the device is mounted with an element formation surface thereof facing a submount for mounting (pg. 4, paragraph [0063]; Figs. 1-9);

21. Regarding claim 21, Hasegawa et al. discloses a diode as described in reference to claim 1, wherein the light-emitting layer (item 16) has a multiple quantum well structure (item 15) formed by alternately stacking a quantum well layer made of group III-V nitride semiconductor not containing As, P and Sb, and a barrier layer made of group III-V nitride semiconductor.

### ***Conclusion***

Applicant's amendment filed 10/14/2008 necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to VERNON P. WEBB whose telephone number is (571)270-3332. The examiner can normally be reached on Monday through Friday, 7:30 am to 5 pm, Eastern.



If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571-272-1760. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lynne A. Gurley/  
Supervisory Patent Examiner, Art  
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Examiner, Art Unit 2811